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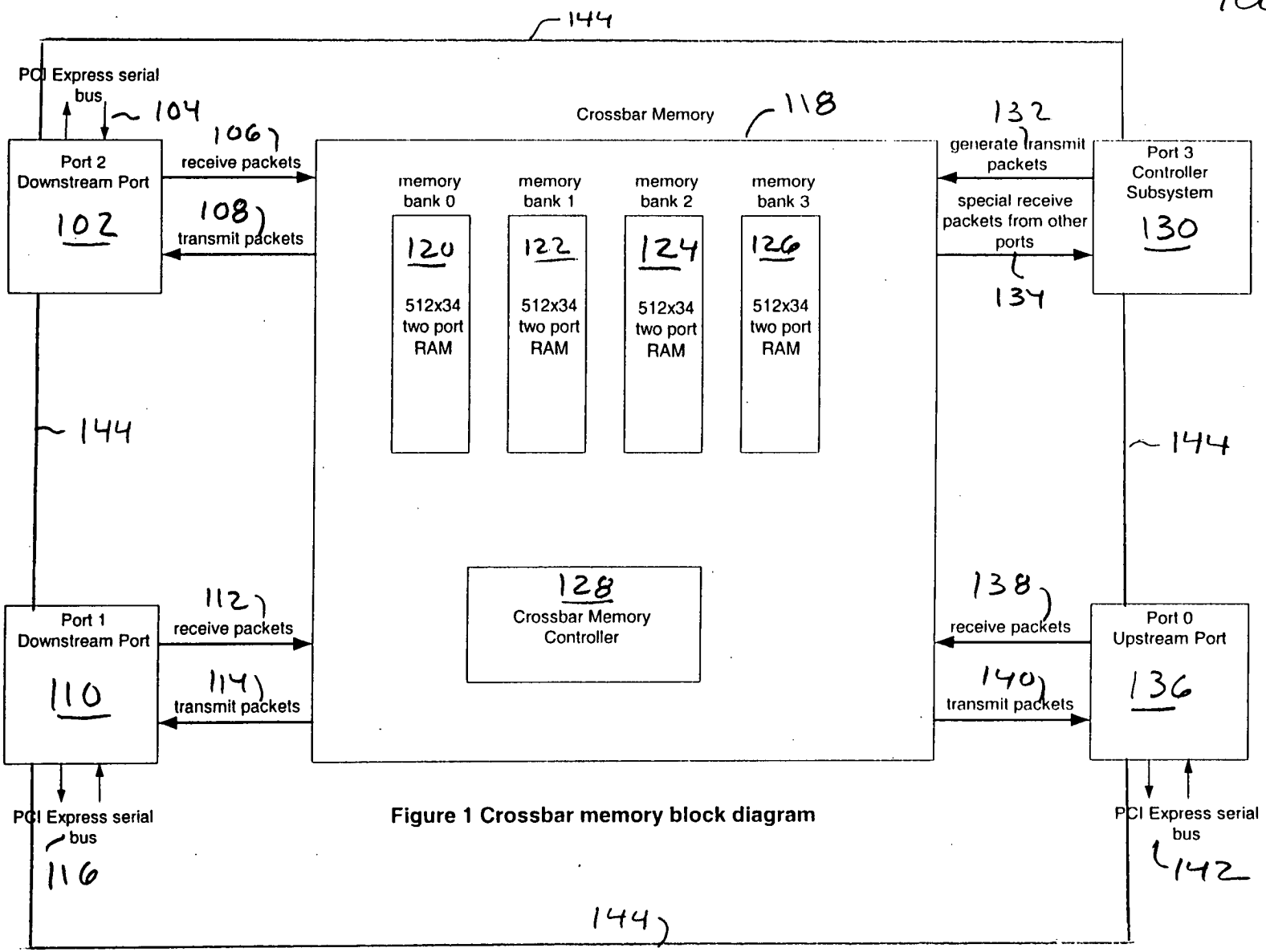

Figure 1 Crossbar memory block diagram

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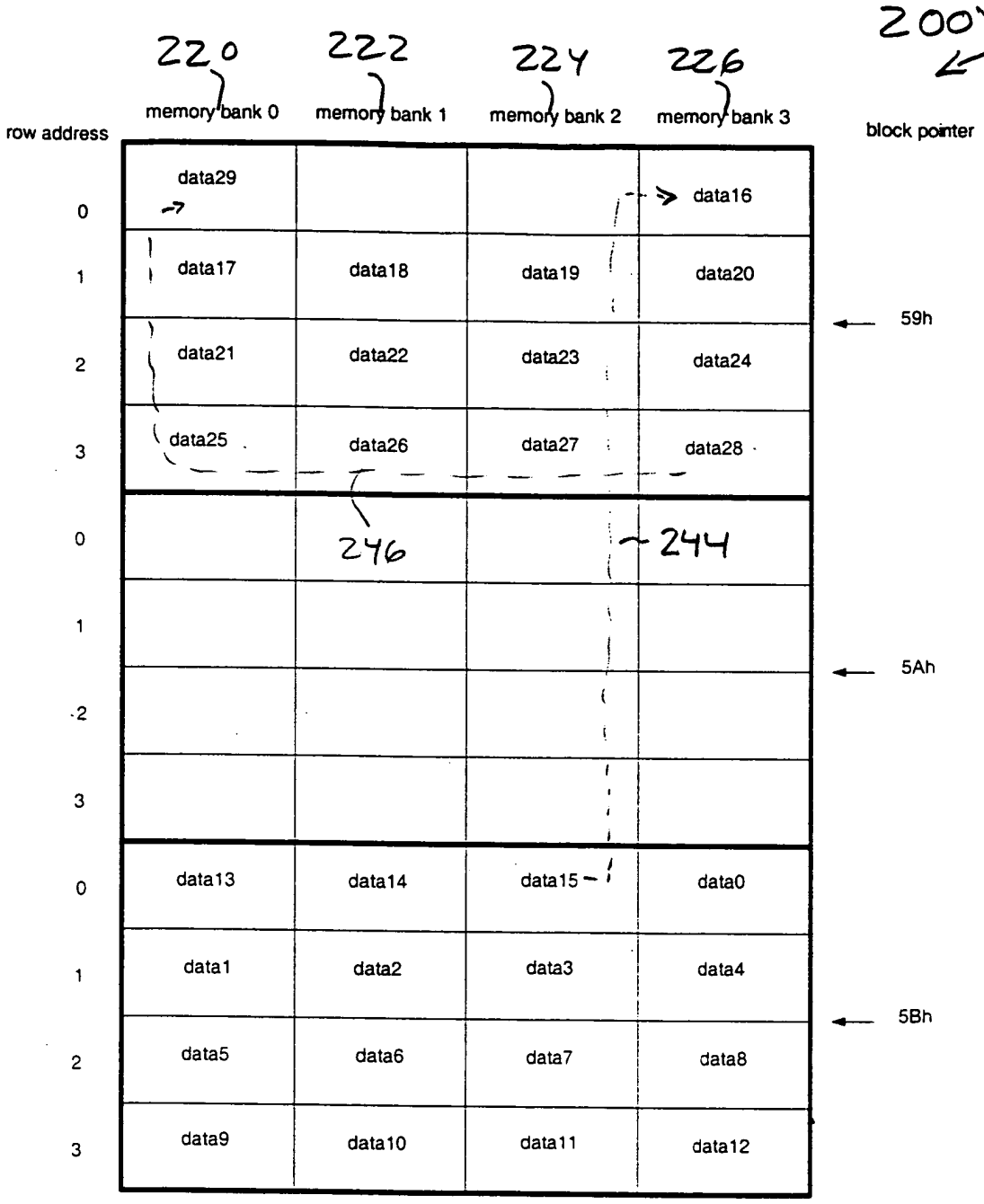

Figure 2 Crossbar memory packet storage

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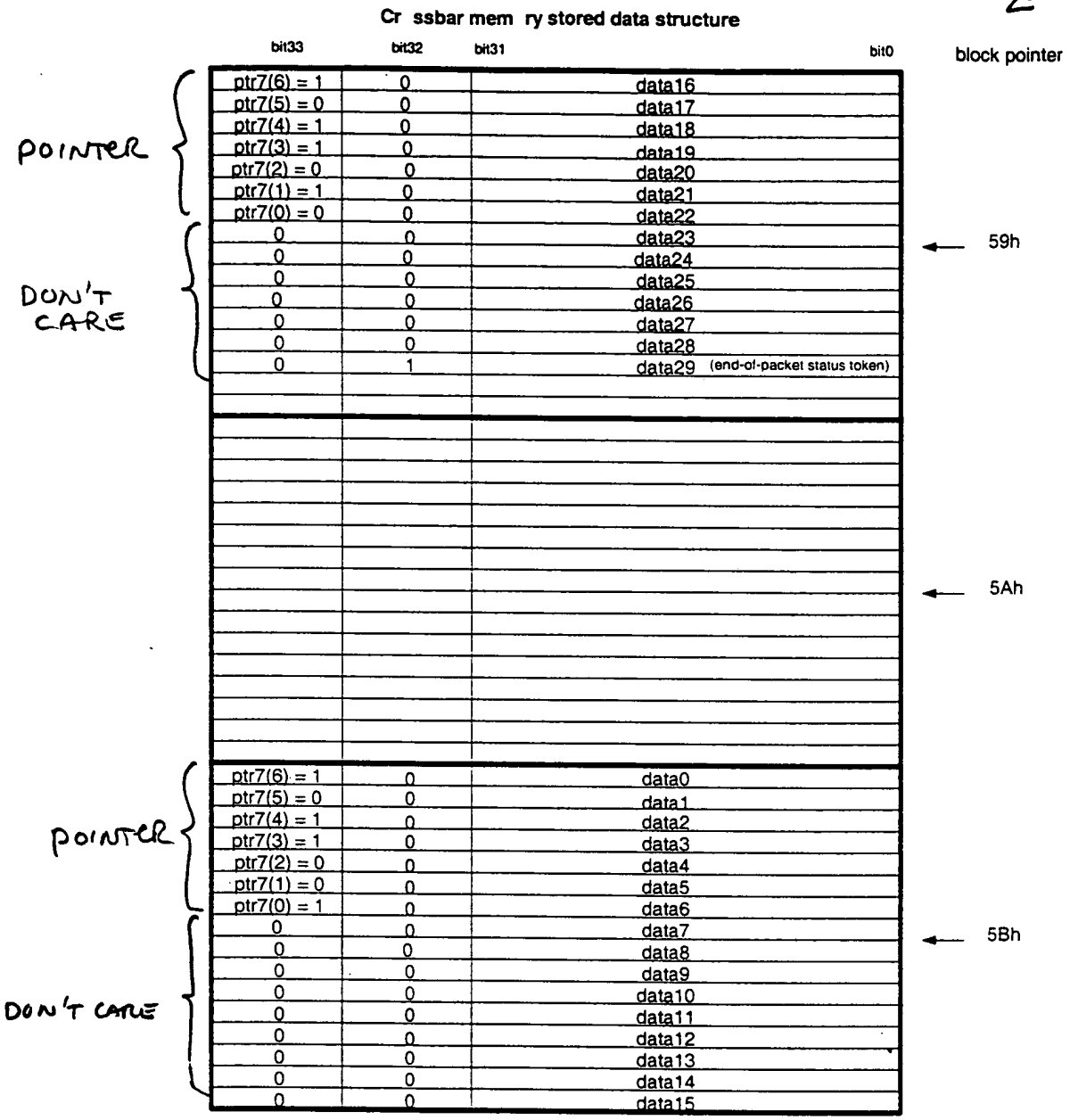

Figure 3 PCI Express packet storage data structure

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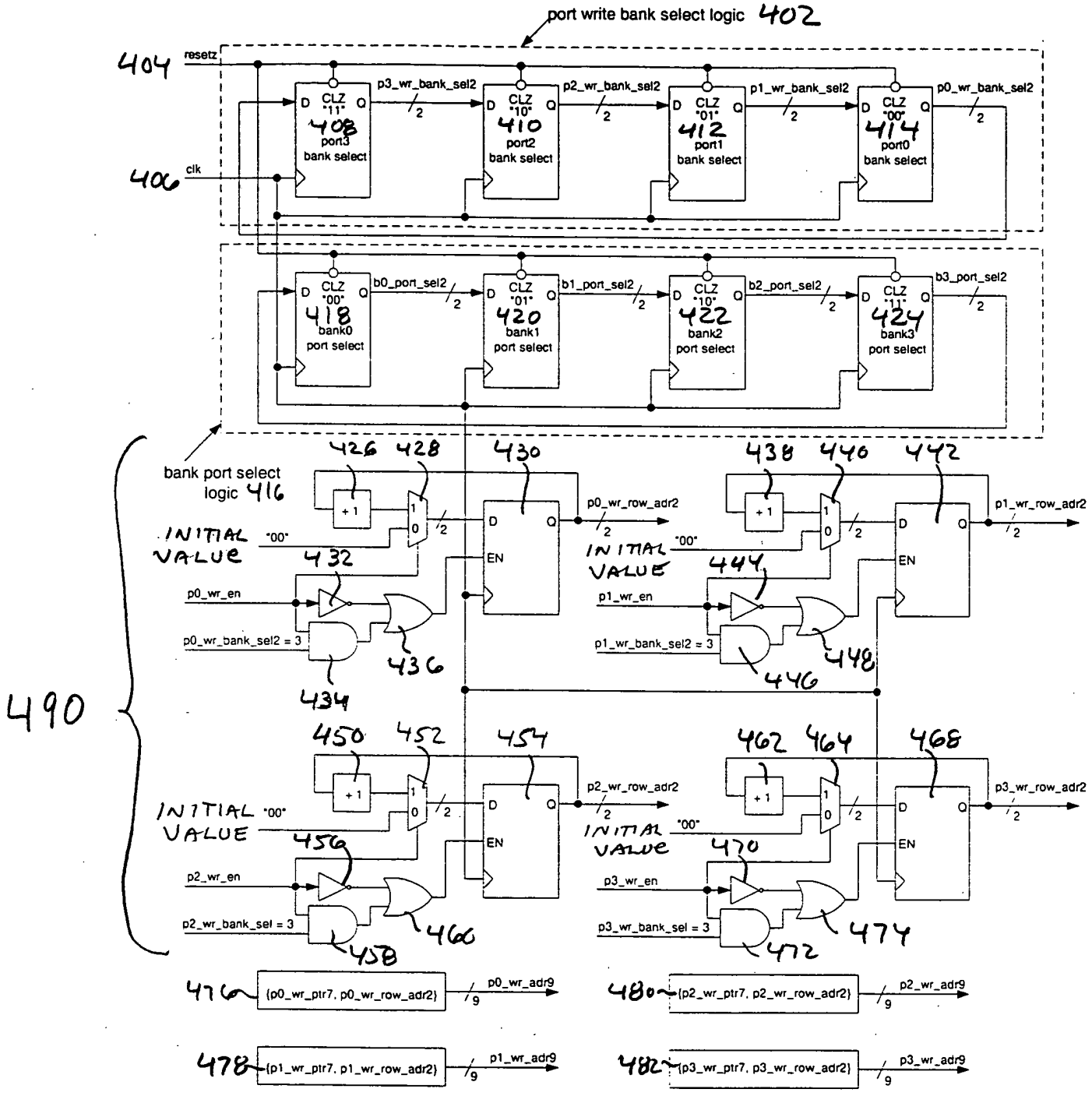

Figure 4 Crossbar memory controller - bank select, port select and write address logic

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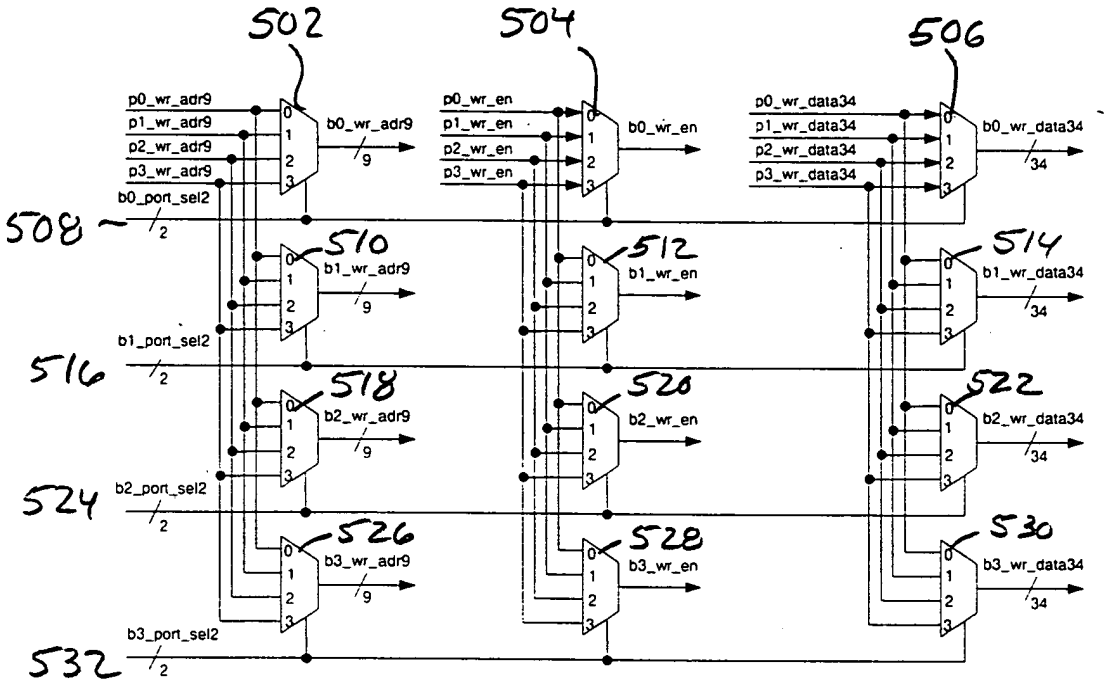

Figure 5 Crossbar memory controller - memory bank write mutiplex logic

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600

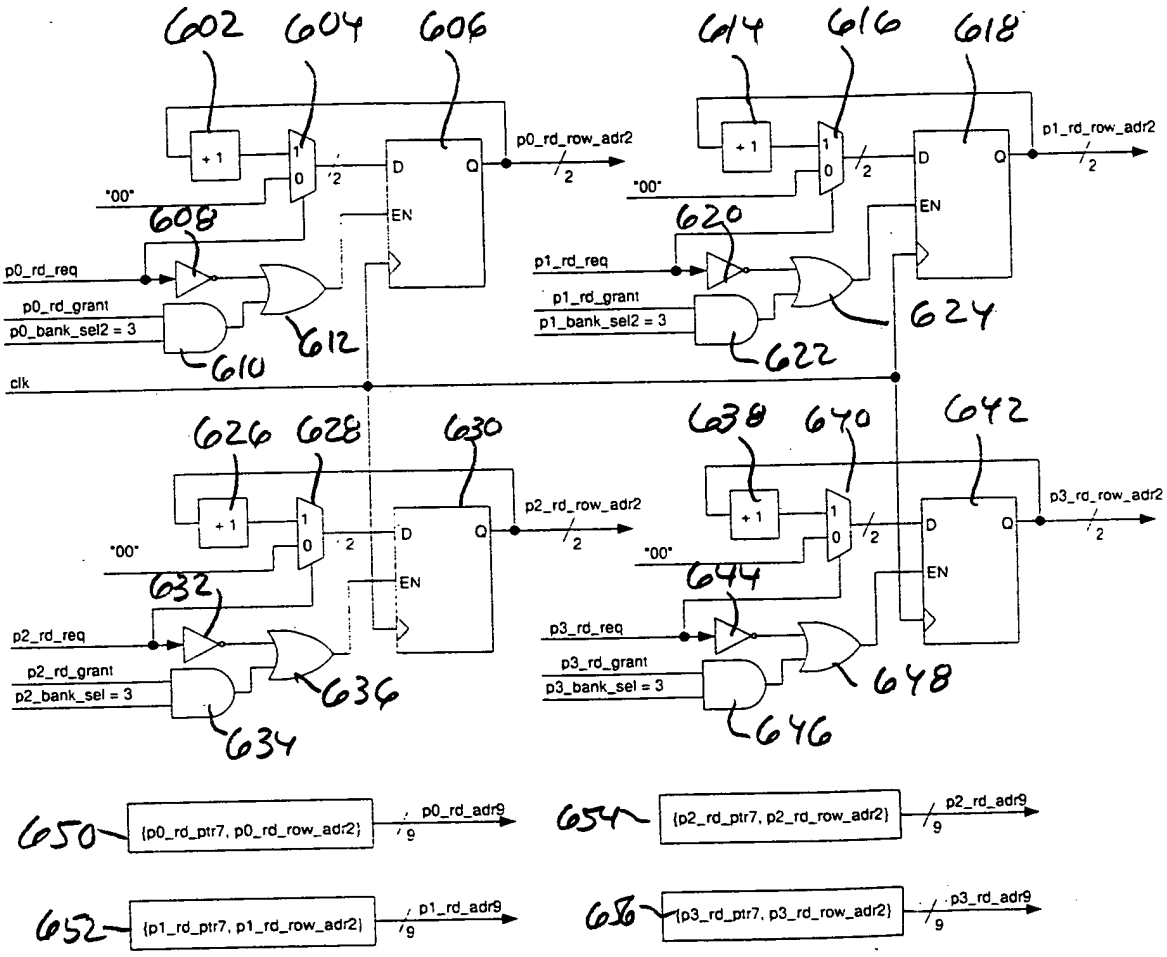

Figure 6 Crossbar memory controller - port read address logic

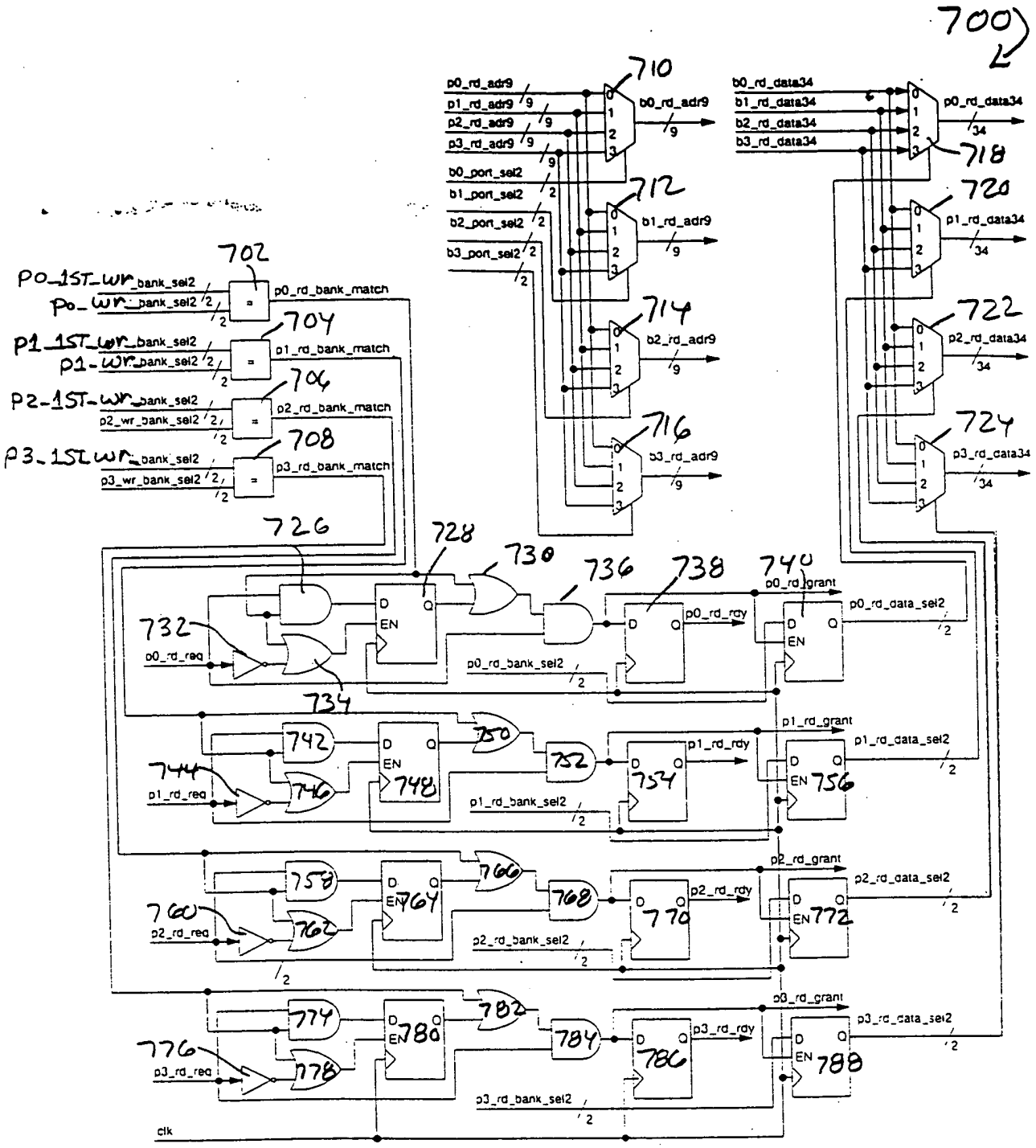

Figure 7 Crossbar memory controller - memory bank read control logic

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800

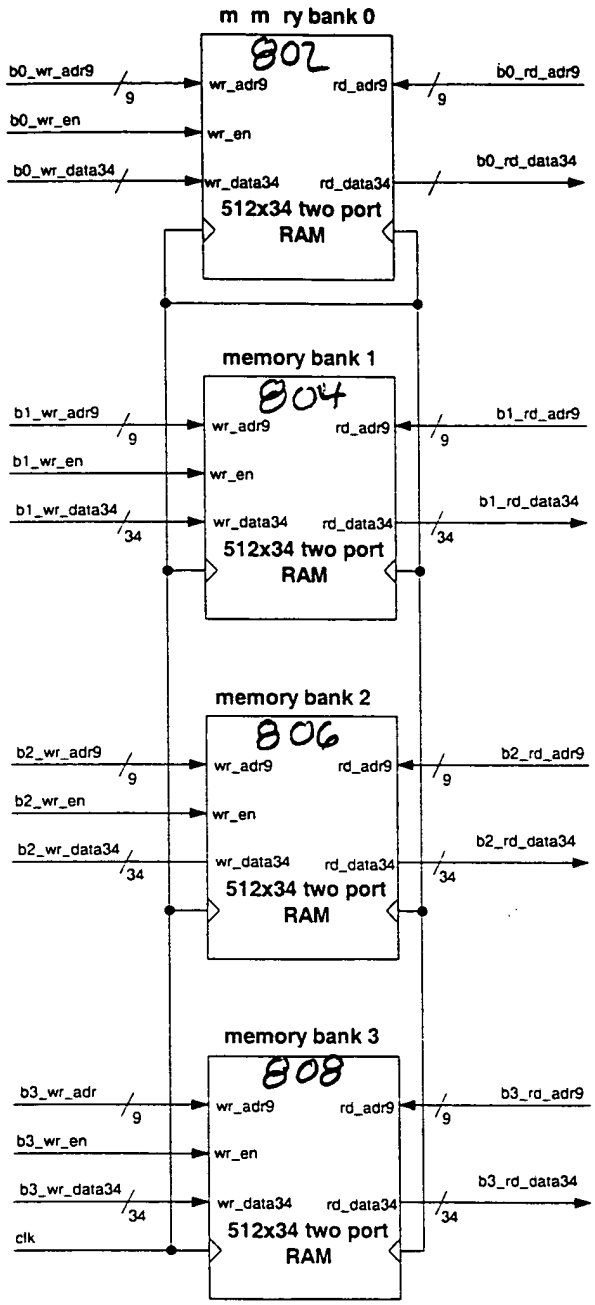

Figure 8 Crossbar memory bank access interface signals

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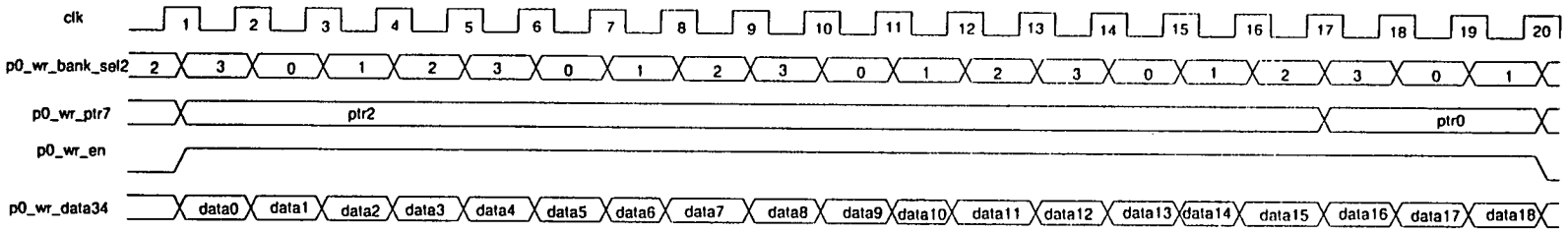

Note:In this example port 0 start writing crossbar memory from memory bank 3

Figure 9 port receive packet write timing diagram

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1000

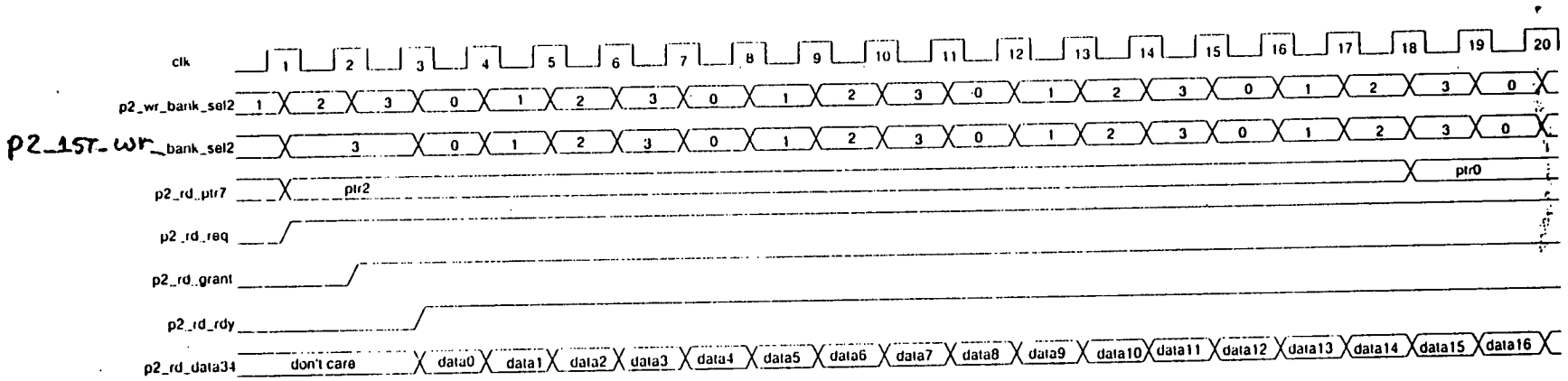

Figure 10 port transmit packet read timing diagram -1

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1109

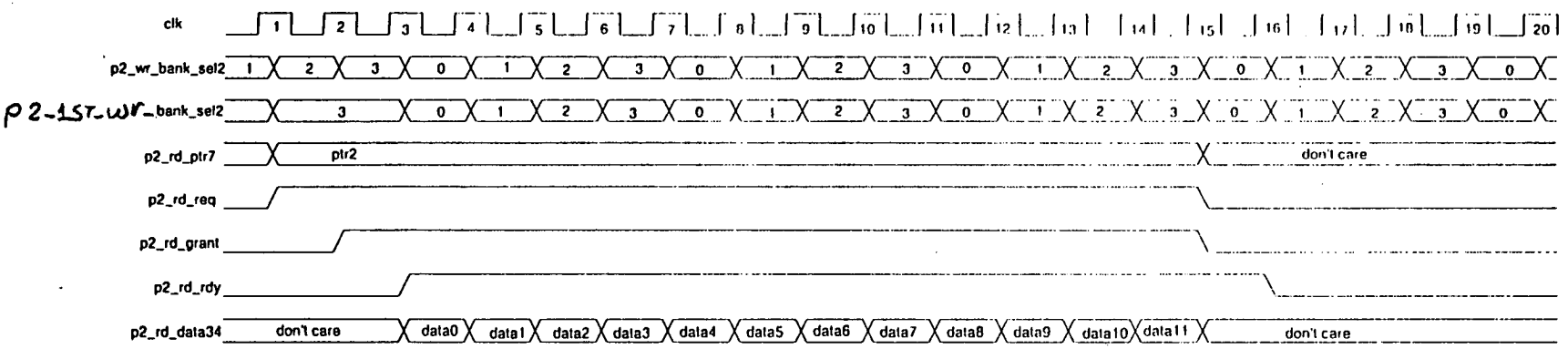

Figure || port transmit packet read timing diagram -2 (shown read termination)

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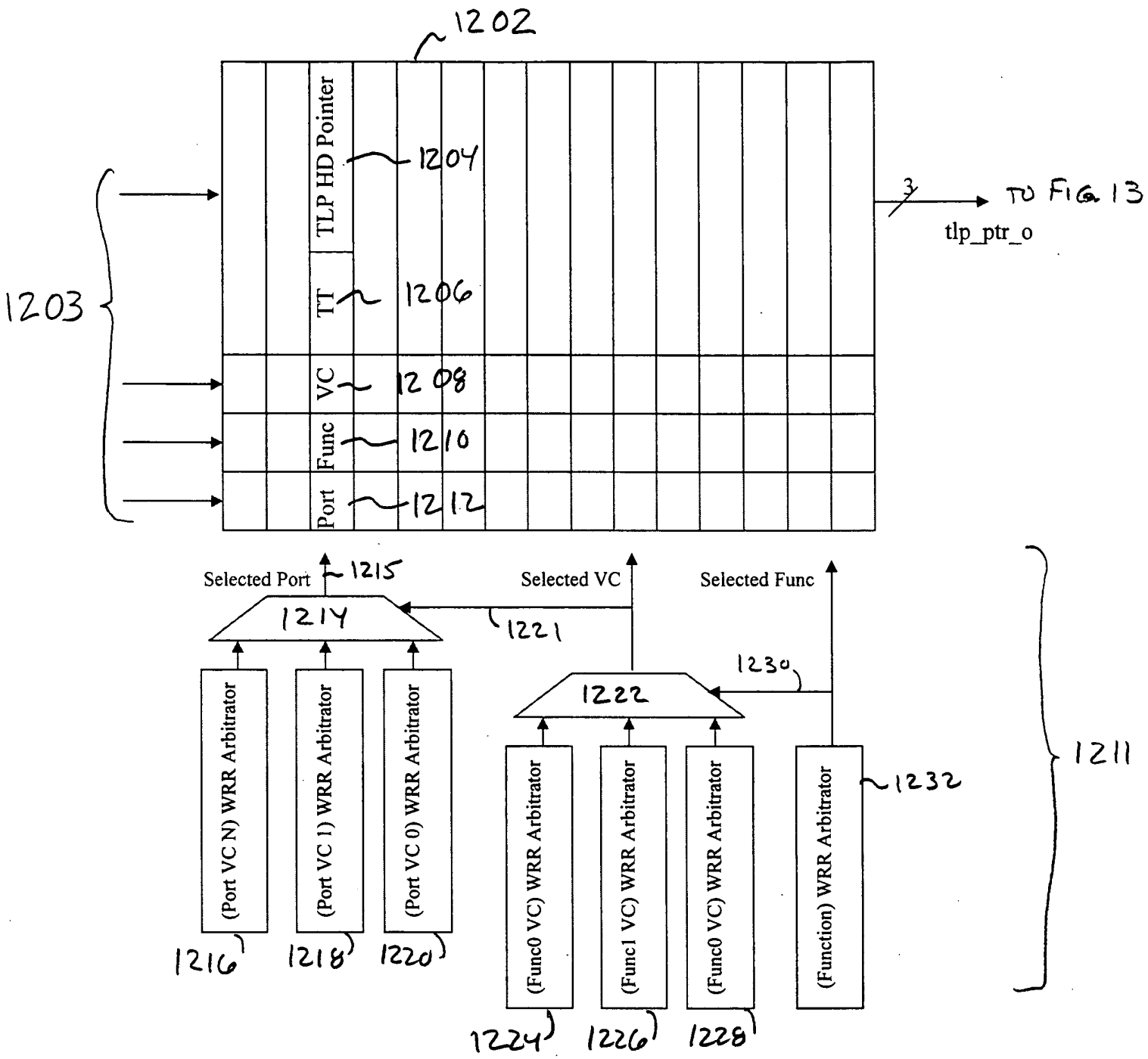

FIG. 12

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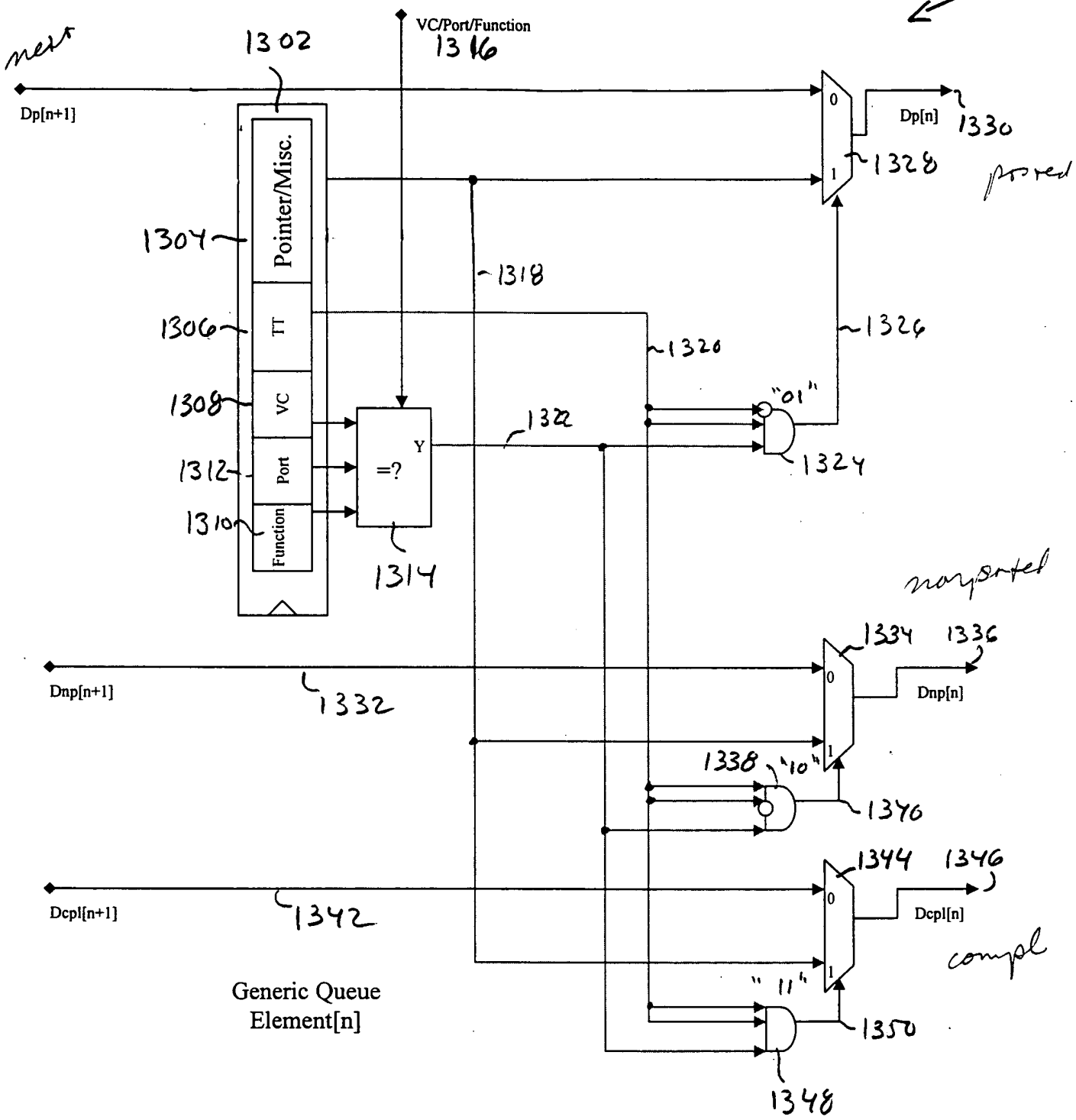

FIG. 13